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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,867	12/30/2004	Fan Yung Ma	2004 LW 2463 US	9311

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EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	**PAPER NUMBER**
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,867	MA, FAN YUNG	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1,2 and 4-7* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of Changes

1. Claims 1-2, and 4-7 are newly rejected see rejections below as necessitated by Applicant's amendment and the IDS submitted 25, September 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, and 4-7 rejected under 35 U.S.C. 102(b) as being anticipated by Kurihara et al. (USPN 6,683,481).

With respect to claim 1, Kurihara et al. discloses, in Figs. 1-7, a detection circuit (circuit of Fig. 6) for monitoring a supply voltages (Fig. 6 monitors the supply voltage IN, which corresponds to a DC supply voltage, see Fig. 1, also see Col. 11 lines 11-13 and Col. 15 lines 17-20 (i.e. Fig. 6 is only different from Fig. 2 in the control circuit 8)) the circuit comprising:

"a comparator (2) for generating a shortfall signal (N2) indicative of a shortfall of the supply voltage in relation to a reference voltage (When IN falls lower than V6 (i.e. shortfall condition of the supply voltage) N2 is output as a "high" signal, see Figs. 5A

and 5B, also see Col. 12 lines 31-3.), the shortfall signal being a current signal (it can be seen that N2 is output as a voltage signal, however it is inherent that all voltages have a current in that voltage equals current multiplied by resistance (i.e. V=I*R), thus the voltage of the signal N2 inherently has a current and therefore is inherently a "current signal") having a value which varies proportionally with the shortfall of the supply voltage in relation to the reference voltage (it can be seen in Figs. 5A and 5B that the value of N2 high while IN is lower than V6. Thus N2's value varies "proportionally to" the shortfall of the supply voltage in relation to the reference voltage in that it is activated (i.e. has a high value) proportionally to the amount of time IN is lower than V6. Therefore to due to the broadest reasonable interpretation N2's value varies proportionally to the shortfall of IN.) and

an integrator (3) for time-integrating the shortfall signal to form an integrated signal (3 clearly time integrates N2, and outputs the time integrated signal as V3. See Fig. 5B and 5C, also see Fig. 7B), wherein the undervoltage detection circuit is arranged to use the integrated signal to generate a reset signal for resetting a microprocessor (Fig. 9 outputs FO, which is responsive to the integrated signal V3 input to 8A of Fig. 9. It can be seen that FO is output to microprocessor 101 of Fig. 1 and the operation of 101 is changed (i.e. reset, and 101 outputs CNT) according to the FO signal (see Col. 11 lines 26-30. Thus 101 is reset by FO.)."

With respect to claim 2, Kurihara et al. discloses, a circuit according to claim 1 further including "a discriminator circuit for receiving the integrated signal (5C is a discriminator that receives the integrated signal N41 (i.e. N41 is effective V3 since N41

is buffered by 4C)) and at least one further output of the comparator (it can be seen that N42 is an additional output signal that corresponds to an output of 2, since V3 is effectively the integrated output of N2, and N42 is simply an inverted version of N2), and generating a reset signal (FO) using the integrated signal and the at least one further output (FO is generated responsive to N41 and N42)."

With respect to claim 4, Kurihara et al. discloses, a circuit comprising:

"microprocessor circuitry (10.1 of Fig. 1);

a undervoltage detection (UVD) circuit (Fig. 6) that includes a comparator (2) for generating a shortfall signal (N2) indicative of a shortfall of the supply voltage (IN) in relation to a reference voltage (N2 is output when the supply voltage IN falls lower than reference voltage V6 see Figs. 5A and 5B), the shortfall signal being a current signal (it can be seen that N2 is output as a voltage signal, however it is inherent that all voltages have a current in that voltage equals current multiplied by resistance (i.e. V=I*R), thus the voltage of the signal N2 inherently has a current and therefore is inherently a "current signal") having a value which varies proportionally with the shortfall of the supply voltage in relation to the reference voltage (it can be seen in Figs. 5A and 5B that the value of N2 high while IN is lower than V6. Thus N2's value varies "proportionally to" the shortfall of the supply voltage in relation to the reference voltage in that it is activated (i.e. has a high value) proportionally to the amount of time IN is lower than V6. Therefore to due to the broadest reasonable interpretation N2's value varies proportionally to the shortfall of IN.) and an integrator (3) for time-integrating the shortfall signal to form an integrated signal (3 integrates N2 to produce integrated signal

V3) wherein the undervoltage detection circuit is arranged to generate a reset signal for resetting a microprocessor (V3 is a reset signal that is output by the undervoltage detection circuit to which reset signal 8A outputs signal FO to reset microprocessor 101 according to V3.) and

reset means (8A) arranged to receive the reset signal output by the UVD circuit and according to its value to initiate a reset of the microprocessor circuit (circuit 8A of Fig. 9 outputs FO, which is responsive to the integrated signal V3 input to 8A of Fig. 9. It can be seen that FO is output to microprocessor 101 of Fig. 1 and the operation of 101 is changed (i.e. reset, and 101 outputs CNT) according to the FO signal (see Col. 11 lines 26-30. Thus 101 is reset by FO.)."

With respect to claim 5, Kurihara et al. discloses in Fig. 5, a method including:

"generating a shortfall signal (N2) indicative of a shortfall of the supply voltage (IN) in relation to a reference voltage (N2 is generated at the output of 2 as a high signal when the supply voltage IN falls lower than V6) the shortfall signal being a current signal (it can be seen that N2 is output as a voltage signal, however it is inherent that all voltages have a current in that voltage equals current multiplied by resistance (i.e. V=I*R), thus the voltage of the signal N2 inherently has a current and therefore is inherently a "current signal") having a value which varies proportionally with the shortfall of the supply voltage in relation to the reference voltage (it can be seen in Figs. 5A and 5B that the value of N2 high while IN is lower than V6. Thus N2's value varies "proportionally to" the shortfall of the supply voltage in relation to the reference voltage in that it is activated (i.e. has a high value) proportionally to the amount of time IN is

lower than V6. Therefore to due to the broadest reasonable interpretation N2's value varies proportionally to the shortfall of IN.);

time-integrating the shortfall signal to form an integrated signal (3 time integrates shortfall signal N2 to produce integrated signal V3), and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor ()."

With respect to claim 6, Kurihara et al. discloses, "the method of claim 5 and further comprising resetting the microprocessor with the reset signal (Fig. 9 outputs FO, which is responsive to the integrated signal V3 input to 8A of Fig. 9. It can be seen that FO is output to microprocessor 101 of Fig. 1 and the operation of 101 is changed (i.e. reset, and 101 outputs CNT) according to the FO signal (see Col. 11 lines 26-30. Thus 101 is reset by FO.)."

With respect to claim 7, Kurihara et al. discloses, the circuit according to claim 4, wherein the UVD circuit further includes "a discriminator circuit for receiving the integrated signal (5C is a discriminator that receives the integrated signal N41 (i.e. N41 is effective V3 since N41 is buffered by 4C)) and at least one further output of the comparator (it can be seen that N42 is an additional output signal that corresponds to an output of 2, since V3 is effectively the integrated output of N2, and N42 is simply an inverted version of N2), and generating a reset signal (FO) using the integrated signal and the at least one further output (FO is generated responsive to N41 and N42)."

Response to Arguments

Applicant's arguments with respect to claims 1-2, and 4-7 have been considered but are moot in view of the new ground(s) of rejection.

With respect to claims 1-2, and 4-7 as rejected under Kurihara et al. it can be seen that all of the recited limitations of claims 1-2 and 4-7 have been addressed in the above rejections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fig. 9 of Shimoda (USPN 6,188,266) discloses and under voltage detecting comparator, which outputs to an integrator.

Figs. 5 and 6 of Hoang (USPN 5,497,112) disclose a under voltage detecting comparator that outputs a shortfall signal (PUNDER) of a detected supply voltage signal. In Fig. 6 Hoang discloses an integrator (T76-T78), which outputs to a discriminator (N3). However, Hoang's integrator integrates the over voltage detection signal to insure that the supply voltage has returned to a normal supply range.

Allowable Subject Matter

Claims 3 and 8 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 3, there was no prior art found that taught the used of a control signal control switches of the discriminator circuit as recited in claim 3. Also, there was no prior art found that provided motivation for combining Yoshimura or Kurihara et al. with a switched discriminator that accepts signals output form a comparator, and an integrated signal that is generated form a different output of a comparator. Thus claim 3 is allowable, and claim 8 is allowed based on the same reasoning as claim 3.

Claims 9 and 10 are allowed

With respect to claim 9, there is no cited art that teaches the use of a control signal control switches of the discriminator circuit as recited in claim 9. Also, there is no cited art that provides motivation for combining Yoshimura or Kurihara et al with a switched discriminator that accepts signals output form a comparator, and an integrated signal that is generated form a different output of a comparator. Thus claim 9 is allowed, and claim 10 is allowed based on the same reasoning as claim 3.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Additionally, Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 25 September 2006 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b) and

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
January 10, 2007

LINH MY NGUYEN
PRIMARY EXAMINER